AMENDMENT TO THE SPECIFICATION

Please amend the specification by marked up replacement paragraph(s) as follows. The paragraph numbering corresponds to the published application (No. 2004/0086059).

Please replace paragraph [101] with the following:

-- FIG. 7 is a graph showing performance between codes utilizing unrestricted parity check matrix (H matrix) versus restricted H matrix of FIG. 6. The graph shows the performance comparison between two LDPC codes: one with a general parity check matrix and the other with a parity check matrix restricted to be lower triangular (i.e., restricted H matrix) to simplify encoding. The modulation scheme, for this simulation, is 8-PSK. The performance loss is within 0.1 dB. Therefore, the performance loss is negligible based on the restriction of the lower triangular H matrices, while the gain in simplicity of the encoding technique is significant. Accordingly, any parity check matrix that is equivalent to a lower triangular or upper triangular under row and/or column permutation can be utilized for the same purpose.

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Please replace paragraph [131] with the following:

-- Next, the decoder 305, per step ~~1205~~ 1005, outputs *a posteriori* probability information (FIG. 12C), such that:

$$a_n = u_n + \sum_j w_{k_j \to n} \text{ .} \text{--}$$

Please replace paragraph [132] with the following:

-- Per step 1007, it is determined whether all the parity check equations are satisfied. If these parity check equations are not satisfied, then the decoder 305, as in step 1009, re-derives 8-PSK bit metrics and channel input u_n. Next, the bit node is updated, as in step 1011. As shown in FIG. 14C, the incoming messages to the bit node n from its d_v adjacent check nodes are denoted by $w_{k_1 \to n}, w_{k_2 \to n}, \ldots, w_{k_{dv} \to n}$. The outgoing messages from the bit node n are computed back to d_v adjacent check nodes; such messages are denoted by $v_{n \to k_1}, v_{n \to k_2}, \ldots, v_{n \to k_{dv}}$, and computed as follows:

$$v_{n \to k_i} = u_n + \sum_{j \neq i} w_{k_j \to n} \text{ .}$$

In step 1013, the decoder 305 outputs the hard decision (in the case that all parity check equations are satisfied):

$$\hat{c}_n = \begin{cases} 0, & a_n \geq 0 \\ 1, & a_n < 0 \end{cases} \qquad \text{Stop if } H\hat{c}^T = 0 \text{ .--}$$

Please replace paragraph [167] with the following:

-- The computer system 1600 can send messages and receive data, including program code, through the network(s), network link 1619, and communication interface 1617. In the Internet example, a server (not shown) might transmit requested code belonging to an application program for implementing an embodiment of the present invention through the network 1625, local network 1621 and communication interface 1617. The processor 1603 may execute the transmitted code while being received and/or store the code in storage device ~~169~~ 1609, or other non-volatile storage for later execution. In this manner, computer system 1600 may obtain application code in the form of a carrier wave. --